

FEATURES

- 500 MHz to 50 GHz
- Low-Profile Package
- Input Regulators for Improved Stability
 Versus Power Supply Variations
- 16 Bit Tuning Resolution

DESCRIPTION

YIG TUNED BANDREJECT FILTERS WITH COMMERCIAL SERIAL DRIVERS SM SERIES



MICRO LAMBDA YIG Filters, model types MLFR, MLFRD and MLUN-Series are available with integrated serial driver circuits.

MICRO LAMBDA drivers eliminate the need for customers to design or develop their own driver circuits and sophisticated test and alignment procedures. Integrating a driver at MICRO LAMBDA's factory ensures that peak performance will be achieved at the time of manufacture. Alignment and compensation with the particular YIG filter can be maximized down to the component level.

All drivers in this series provide input voltage regulators, and compensation circuits to improve frequency drift.

COMMERCIAL SERIAL DRIVERS	
DRIVER INPUT & RESPONSE	SPECIFICATION (0 to +65 deg. C)
Tuning Command	Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency
Tuning Resolution	16 BIT Positive Logic (Fmax-Fmin)/65,535 Bit Resolution
Tuning Accuracy (excluding hysteresis)	See Table
Tuning Speed	5 mS for 1 GHz step to within ±10 MHz.
Main Driver Inputs Supply Voltage & Current (P1-6) (P1-5) Supply Voltage Pushing Supply Voltage Ripple Ground (P1-4, 12) YIG Heater Voltage & Current (P1-7, 8)	+15 V ± .5 V @ Filter Tuning Current +50 mA, Max. -15 V ± .5 V @ 50 mA ± 100 kHz, Max. @ ± .5 Vdc 10 mV Ripple Pk-Pk from 2 kHz to 3 MHz Chassis Ground +24 Vdc ±4 Vdc @ 300 - 750 mA surge for 2 seconds, 100 - 150 mA steady state depending on filter type. Polarity independent : ±12 Vdc or ±15 Vdc acceptable
Digital Interface (P1-1, 2, 3, 4)	The MLWI digital driver interface is a standard 3-wire connection compat- able with SPI/QSPI/MICROWIRE interfaces. The 3-wire serial interface will operate in a 5V or 3.3V logic system. The chip-select input (SELECTn) frames the serial data loading at the data input pin (DATA). Immediately following SELECTn's high-to-low transition, the data is shift- ed synchronously and latched into the input register on the rising edge of the serial-clock input (CLOCK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on SE- LECTn's low-to-high transition (Figure 2). Note that if SELECTn does not remain low during the entire 16 CLOCK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

SM-SERIES — CONT.

YIG Tuned Bandreject Filters with Commercial Serial Drivers

Power-On Reset

The MLWI digital driver has a power-on reset circuit to set the DAC's output to OV(F-min) in unipolar mode when VDD is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after power loss.

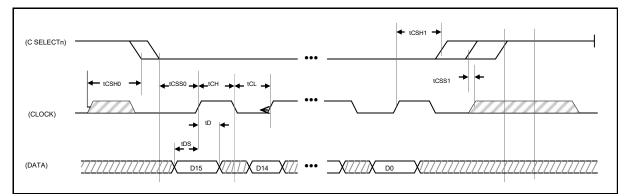
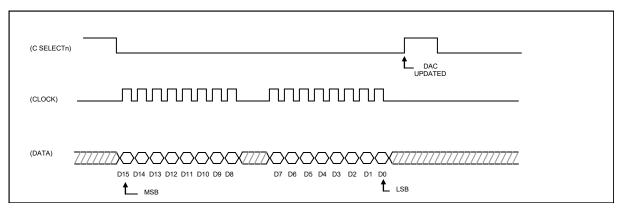
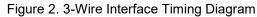


Figure 1. Timing Diagram





TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX	UNITS
CLOCK Frequency	fCLK		10	MHz
CLOCK Pulse Width High	tCH		45	ns
CLOCK Pulse Width Low	tCL		45	ns
CSn Low to CLOCK High Setup	tCSS0		45	ns
CSn High to CLOCK High Setup	tCSS1		45	ns
CLOCK High to CSn Low Hold	tCSH0		30	ns
CLOCK High to CSn High Hold	tCSH1		45	ns
DATA to CLOCK High Setup	tDS		40	ns
DATA to CLOCK High Hold	tDH		0	ns
VDD High to CSn Low (power-up delay)			20	μs

Micro Lambda Wireless, Inc. - 46515 Landing Parkway, Fremont California 94538 * Phone (510) 770-9221 * Fax (510) 770-9213



YIG TUNED BANDREJECT FILTERS W/ COMMERCIAL SERIAL DRIVERS SM SERIES – CONTINUED

Band Reject Filters with Positive Input Serial Drivers (0° C to +65° C)

Model	Frequency	3 dB	40 dB	Accuracy	Current	Current	Outline
Number	GHz	Bandwidth (MHz)	Bandwidth (MHz)	(MHz) *	+15 V (mA)	-15 V (mA)	Drawing
MLFR-0102SM	1.0 to 2.0	100	10	+/- 5	250	50	99-0021-177
MLFR-0204SM	2.0 to 4.0	125	15	+/- 7	350	50	99-0021-177
MLFR-0408SM	4.0 to 8.0	150	20	+/- 10	550	50	99-0021-177
MLFR-0812SM	8.0 to 12.4	150	25	+/- 12	750	50	99-0021-177
MLFR-1218SM	12.4 to 18.0	150	25	+/- 12	1050	50	99-0021-177
MLFR-0502SM	0.50 to 2.0	100	5 @ 30dB	+/- 5	250	50	99-0021-177
MLFR-0206SM	2.0 to 6.0	150	20	+/- 10	450	50	99-0021-177
MLFR-0208SM	2.0 to 8.0	150	15	+/- 14	550	50	99-0021-177
MLFR-0212SM	2.0 to 12.0	150	10	+/- 15	750	50	99-0021-177
MLFR-0218SM	2.0 to 18.0	150	10	+/- 25	1050	50	99-0021-177
MLFR-0220SM	2.0 to 20.0	150	5	+/- 25	1050	50	99-0021-177
MLFR-0418SM	4.0 to 18.0	150	10	+/- 20	1050	50	99-0021-177
MLFR-160418SM	4.0 to 18.0	150	30	+/- 20	1050	50	99-0021-177
MLFR-0618SM	6.0 to 18.0	150	25	+/- 18	1050	50	99-0021-177
MLFR-160618SM	6.0 to 18.0	150	40	+/- 20	1050	50	99-0021-177
MLFR-0818SM	8.0 to 18.0	150	35	+/- 18	1050	50	99-0021-177
MLFR-160818SM	8.0 to 18.0	150	50	+/- 18	1050	50	99-0021-177

Ultra Notch Band Reject Filters with Positive Input Serial Drivers (0° C to +65° C)

Model	Frequency	3 dB	60 dB	Accuracy	Current	Current	Outline
Number	GHz	Bandwidth (MHz)	Bandwidth (MHz)	(MHz) *	+15 V (mA)	-15 V (mA)	Drawing
MLUN-0305SM	.35 to .52	50	4 @ 30dB	+/- 2	100	50	99-0021-175
MLUN-0503SM	.50 to 3.0	80	6@ 40dB	+/- 5	250	50	99-0021-175
MLUN-0206SM	2.0 to 6.0	120	20	+/- 10	450	50	99-0021-175
MLUN-0618SM	6.0 to 18.0	175	40	+/- 18	1050	50	99-0021-177
MLUN-0218SM	2.0 to 18.0	175	10	+/- 25	1050	50	99-0021-177
MLUN-0220SM	2.0 to 20.0	175	10	+/-25	1050	50	99-0021-177

* Accuracy includes frequency drift and linearity errors over the temperature range.

** Contact Factory

Micro Lambda Wireless, Inc. - 46515 Landing Parkway, Fremont California 94538 * Phone (510) 770-9221 * Fax (510) 770-9213

